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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/888,562	06/26/2001	David I. Poisner	2207/11507	9411

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EXAMINER	
BUTLER, DENNIS	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/888,562	POISNER ET AL.
	Examiner	Art Unit
	Dennis M. Butler	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-13 and 15-21* is/are rejected.

7)☒ Claim(s) *8 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This action is in response to the application filed on June 26, 2001. Claims 1-21 are pending. Applicant's Declaration is not present in the file. Applicant submitted a letter dated December 17, 2001 that states that a Declaration was submitted. However, it is missing from the file. Applicant is requested to submit a copy of the Declaration in response to this office action.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 21 is indefinite because it is dependent on non-existent claim 22 and it is unclear how it relates to the existing claims.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-4, 7, 9-11, 15-16 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Gulick, U. S. Patent 6,195,749.

Per claim 1:

A) Gulick teach the following claimed items:

1. a CPU with Microprocessor 100 of figure 1;

2. RAM separate from main memory accessible to the CPU for use as a stack during BIOS processing with Buffer Memory 200 of figure 3 and at column 3, lines 3-10 and 20-38.

Per claims 2-4 and 7:

Gulick describes an address decoder coupled to the CPU and RAM with Memory Access Controller 140 of figure 3 and at column 3, line 56 – column 4, line 19. Gulick describes the CPU executing an instruction to access the stack at column 4, lines 12-19. The stack inherently includes a stack pointer in the CPU for

accessing the stack. Gulick describes BIOS instructions including an instruction setting an operational mode (RAM/initialization or FIFO/normal modes) of the CPU to access the RAM with Configuration Storage Unit 180 of figure 3 and at column 3, line 65 – column 4, line 29.

Per claim 9:

A) Gulick teach the following claimed items:

1. mapping a range of address space to RAM separate from main memory (Buffer 200) at column 3, lines 20-30 and at column 4, lines 8-19;

2. executing BIOS that uses space in the RAM (Buffer 200) for a stack at column 3, lines 3-10 and 20-38.

Per claims 10 and 11:

Gulick describes the CPU executing an instruction to access the stack at column 4, lines 12-19. The stack inherently includes a stack pointer in the CPU for accessing the stack.

Per claim 15:

A) Gulick teach the following claimed items:

1. a CPU with Microprocessor 100 of figure 1;

2. RAM separate from main memory accessible to the CPU for use as a stack during BIOS processing with Buffer Memory 200 of figure 3 and at column 3, lines 3-10 and 20-38;

3. an address decoder coupled to the CPU and RAM with Memory Access Controller 140 of figure 3 and at column 3, line 56 – column 4, line 19 ;

4. the CPU executing an instruction to access the stack at column 4, lines 12-19. The stack inherently includes a stack pointer in the CPU for accessing the stack.

Per claim 16:

Gulick describes the CPU executing an instruction to access the stack at column 4, lines 12-19.

Per claim 20:

A) Gulick teach the following claimed items:

1. the CPU executing an instruction to access the stack at column 4, lines 12-19. The stack inherently includes a stack pointer in the CPU for accessing the stack.

8. Claims 5, 12, 13, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick, U. S. Patent 6,195,749 in view of Yamazaki et al., U. S. Patent 6,038,632.

Per claims 5, 12, 13, 17 and 21:

Gulick teaches the items of claims 1, 3, 7, 9, 15 and 20 as described in the above art rejections. The claims seem to differ from Gulick in that Gulick fails to explicitly teach calling a subroutine from the BIOS, mapping the range of address space above top of memory and dividing the RAM into first and second portions as claimed. Yamazaki teaches that it is known to call a subroutine from the BIOS with figure 10 and at column 12, lines 50-62. It would have been obvious to one having ordinary skill in the art at the time the invention was made to call a

subroutine from the BIOS, as taught by Yamazaki, in order to reduce the initialization time of a computer by initializing the devices in parallel. One of ordinary skill in the art would have been motivated to combine Gulick and Yamazaki because of Yamazaki's suggestion that performing initialization in parallel using a plurality of subroutines reduces initialization time at column 1, lines 30-51, at column 3, lines 8-12 and with figure 10. It would have been obvious for one of ordinary skill in the art to combine Gulick and Yamazaki and because they are both directed to the problem of booting and initializing a computer by executing BIOS and POST routines. Regarding mapping the range of address space above top of memory, Gulick describes mapping a range of address space to RAM (Buffer 200) at column 3, lines 20-30 and at column 4, lines 8-19. Gulick does not explicitly describe the particular address range that the RAM (Buffer 200) is mapped in system memory. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to map the range of address space above top of memory because this address range is not used by main memory and corruption of the main memory by the RAM address space would be avoided. Regarding dividing the RAM into first and second portions where only the first portion is accessible by the address decoder, Gulick describes mapping a range of address space to RAM (Buffer 200) at column 3, lines 20-30 and at column 4, lines 8-19. Gulick does not explicitly describe the particular address range size/space requirements of the BIOS initialization procedure. However, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to map only the range of addresses needed and leave any excess memory of Buffer 200 unmapped because mapping the unused memory would not be necessary and could corrupt address space used by main memory or other devices.

9. Claims 6, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulick, U. S. Patent 6,195,749.

Per claims 6, 18 and 19:

A) Gulick teach the following claimed items:

1. a CPU with Microprocessor 100 of figure 1;

2. a memory controller with Memory Control 114 of figure 1;

3. an I/O controller with LAN Controller 170 of figures 2 and 3;

4. RAM separate from main memory with Buffer Memory 200 of figure 3 and at column 3, lines 3-10 and 20-38;

5. an address decoder coupled to the CPU and RAM with Memory Access Controller 140 of figure 3 and at column 3, line 56 – column 4, line 19;

6. the CPU executing an instruction to access the stack at column 4, lines 12-19. The stack inherently includes a stack pointer in the CPU for accessing the stack.

B) The claims seem to differ from Gulick in that Gulick fails to explicitly teach a multiplexer coupled between the address decoder to enable access to the ram by either the address decoder or at least one functional logic block of the computer as claimed.

C) However, Gulick describes BIOS instructions including an instruction setting an operational mode (RAM/initialization or FIFO/normal modes) of the CPU to access the RAM with Configuration Storage Unit 180 of figure 3 and at column 3, line 65 – column 4, line 29. Therefore, Gulick discloses that Configuration Storage Unit 180 acts as a programmable switch that is used to switch between two modes of using Buffer 200, the RAM/initialization mode or the FIFO/normal mode. Gulick discloses the claimed invention except for explicitly reciting using a multiplexer to enable access to the RAM. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a multiplexer in place of Gulick's Configuration Storage Unit 180, in order to switch between the two modes of using Buffer 200.

10. Claims 8 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 703-305-9663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler

Dennis M. Butler

Primary Examiner

Art Unit 2115